IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

CARLSSON | Atty. Ref.: 2447-14

Serial No. To be Assigned | Group:

Filed: May 2, 2001 | Examiner:

For: MULTI-SERVICE CIRCUIT FOR TELECOMMUNICATIONS

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May 2, 2001

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

PRELIMINARY AMENDMENT

In order to place the above-identified application in better condition for examination, please amend the application as follows:

IN THE CLAIMS

Please cancel claims 28-38.

Please substitute the following amended claims for corresponding claims previously presented. A copy of the amended claims showing current revisions is attached.

1. (Amended) A multi-service circuit which receives information-bearing cells on an external interface, the multi-service circuit being controlled by a processor, the multi-service circuit comprising:

plural service devices handling differing telecommunication services;

a multiplexer/demultiplexer core connected between the plural service devices and the external interface, the core having a downstream side for transmitting cells from the external interface to the service devices and an upstream side for transmitting cells from the service devices to the external interface, the upstream side including an upstream multiplexer and an upstream demultiplexer, the downstream side having a downstream demultiplexer and a downstream multiplexer where are distinct from the upstream multiplexer and upstream demultiplexer,

wherein the downstream demultiplexer serves to route cells received from the external interface either:

(1) to an input of the downstream multiplexer; or

(2) to one of:

(a) a downstream loop back buffer which stores cells routed from the downstream side to the upstream side, and

(b) the processor.

4. (Amended) The apparatus of claim 1, wherein the upstream side has an upstream demultiplexer and an upstream multiplexer, and

wherein the upstream demultiplexer serves to route cells received from the service devices to one of:

(1) a buffering section situated between the upstream demultiplexer and the upstream multiplexer; and

(2) either:

(a) an upstream loop-back buffer, or

(b) the processor.

6. (Amended) The apparatus of claim 4, wherein the upstream multiplexer serves to obtain cells from one of the buffering section and the downstream loop-back buffer, wherein such obtained cells may be sent to the external interface.

16. (Amended) A multi-service circuit which receives information-bearing cells on an external interface, the multi-service circuit being controlled by a processor, the multi-service circuit comprising:

plural service devices handling differing telecommunication services;

a multiplexer/demultiplexer core connected between the plural service devices and the external interface, the core having a downstream side for transmitting cells from the external interface to the service devices and an upstream side for transmitting cells from the service devices to the external interface, the upstream side having an upstream multiplexer and an upstream demultiplexer, and the downstream side including a downstream multiplexer and a downstream demultiplexer,

wherein the upstream demultiplexer serves to route cells received from the service devices to one of:

(1) a buffering section situated between the upstream demultiplexer and the upstream multiplexer; and

(2) either:

(a) an upstream loop-back buffer which routes cells from the upstream side to the downstream side, or

(b) the processor.

18. (Amended) The apparatus of claim 17, wherein the upstream multiplexer serves to obtain cells from one of the buffering section and the downstream loop-back buffer, so that such obtained cells may be sent to the external interface.

39. (Amended) A multi-service circuit which receives ATM cells on an external interface from a modem/transceiver, the multi-service circuit being controlled by a processor, the multi-service circuit being fabricated as a chip and comprising:

plural service devices handling differing telecommunication services;

a multiplexer/demultiplexer core connected between the plural service devices and the external interface, said core including each of a downstream multiplexer, a downstream demultiplexer, an upstream multiplexer and an upstream demultiplexer;

an internal interface connecting the core to the plural service devices; and

wherein, in a downstream direction, the core routes respective cells received from the external interface to: (i) one of the plural service devices via the internal interface, (ii) the processor, and (iii) the external interface;

wherein, in an upstream direction, the core routes cells received from the plural service devices to one of the external interface, to the processor.

REMARKS

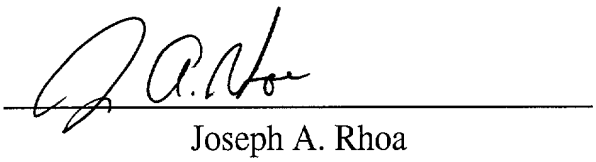
This is a continuation of Serial No. 09/009,635, which was allowed on February 27, 2001. Claims 28-38 have been canceled. Claims 1-27 and 39-41 are now pending.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version With Markings To Show Changes Made**."

It is respectfully submitted that the application is now in condition for allowance.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: 

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please amend the following claims:

1. (Amended) A multi-service circuit which receives information-bearing cells on an external interface, the multi-service circuit being controlled by a processor, the multi-service circuit comprising:

plural service devices handling differing telecommunication services;

a multiplexer/demultiplexer core connected between the plural service devices and the external interface, the core having a downstream side for transmitting cells from the external interface to the service devices and an upstream side for transmitting cells from the service devices to the external interface, the upstream side including an upstream multiplexer and an upstream demultiplexer, the downstream side having a downstream demultiplexer and a downstream multiplexer where are distinct from the upstream multiplexer and upstream demultiplexer,

wherein the downstream demultiplexer serves to route cells received from the external interface either:

(1) to an input of the downstream multiplexer; or

(2) to one of:

(a) a downstream loop back buffer which stores cells routed from the downstream side to the upstream side, and

(b) the processor.

4. (Amended) The apparatus of claim 1, wherein the upstream side has an upstream demultiplexer and an upstream multiplexer, and

wherein the upstream demultiplexer serves to route cells received from the service devices to one of:

(1) a buffering section situated between the upstream demultiplexer and the upstream multiplexer; and

(2) either:

(a) [the] an upstream loop-back buffer, or

(b) the processor.

6. (Amended) The apparatus of claim 4, wherein the upstream multiplexer serves to obtain cells from one of the buffering section and the downstream loop-back buffer [for application], wherein such obtained cells may be sent to the external interface.

16. (Amended) A multi-service circuit which receives information-bearing cells on an external interface, the multi-service circuit being controlled by a processor, the multi-service circuit comprising:

plural service devices handling differing telecommunication services;

a multiplexer/demultiplexer core connected between the plural service devices and the external interface, the core having a downstream side for transmitting cells from the external interface to the service devices and an upstream side for transmitting cells from the service devices to the external interface, the upstream side

having an upstream multiplexer and an upstream demultiplexer, and the downstream side including a downstream multiplexer and a downstream demultiplexer,

wherein the upstream demultiplexer serves to route cells received from the service devices to one of:

(1) a buffering section situated between the upstream demultiplexer and the upstream multiplexer; and

(2) either:

(a) an upstream loop-back buffer which routes cells from the upstream side to the downstream side, or

(b) the processor.

18. (Amended) The apparatus of claim 17, wherein the upstream multiplexer serves to obtain cells from one of the buffering section and the downstream loop-back buffer [for application], so that such obtained cells may be sent to the external interface.

39. (Amended) A multi-service circuit which receives ATM cells on an external interface from a modem/transceiver, the multi-service circuit being controlled by a processor, the multi-service circuit being fabricated as [an] a chip and comprising:

plural service devices handling differing telecommunication services;

a multiplexer/demultiplexer core connected between the plural service devices and the external interface, said core including each of a downstream multiplexer, a downstream demultiplexer, an upstream multiplexer and an upstream demultiplexer;

an internal interface connecting the core to the plural service devices; and

wherein, in a downstream direction, the core routes respective cells received from the external interface to: (i) [to] one of the plural service devices via the internal interface, (ii) [to] the processor, and (iii) [to] the external interface;

wherein, in an upstream direction, the core routes cells received from the plural service devices [via the internal interface and the processor] to one of the external interface, to the processor, and to the internal interface.